

# Justin Reina

[justinmreina@gmail.com](mailto:justinmreina@gmail.com)

[justinreina.com/portfolio](http://justinreina.com/portfolio) (LinkedIn)

11809 Nevers Rd  
Snohomish, WA 98290  
(425)760-7291

## THESIS

Seeking full-time employment in embedded firmware development and related activities.

## EDUCATION

<b>University of Washington</b> Seattle, WA	<i>Cumulative GPA: 3.52</i>
M.S. Electrical Engineering (VLSI)	<i>(hired before completion) 100/117 cr</i>
B.S. Electrical Engineering ( <i>Embedded Design, Control Systems, Analog Design</i> )	<i>Cumulative GPA: 3.30</i>
B.S. Mechanical Engineering ( <i>System Dynamics</i> )	<i>Dec 2009</i>
<b>Everett Community College (EVCC)</b> Everett, WA	<i>Cumulative GPA: 3.37</i>
	<i>Jun 2006</i>

## WORK EXPERIENCE

**Intel Labs** (*Firmware Engineer, Research Scientist*) Jun '11 to Sep '16

Sole firmware engineer for a battery-powered RFID tag for government vehicle tolling in Brazil. Device supports a 3-year battery life and has been deployed in high volumes to the Brazilian government.

Generated a derivative version of the RFID tag supporting a new Intel MCU architecture (D1000), building successfully Intel's first product on the D1000 architecture. Additionally hand-built the IDE tooling (Eclipse) for D1000 development which then became used in the first product release as well.

Both tags featured full physical-layer and protocol implementations on-the-metal, and were certified for ISO-18000:6C, Siniav and Artesp protocol compliance.

**Intel Labs Seattle** (*Firmware Engineer, Research Scientist*) Sep '10 to Jun '11

Successful porting and generation of Passive RFID firmware (WISP) into Active RFID framework for generation of the Brazil Tolling Tag.

**Intermec Technologies** (*RF Test Automation Engineer*) Summer 2008

<i>Task</i>	<i>Results</i>
<ul style="list-style-type: none"><li>Design of RF test system</li><li>802.11/RF competency</li><li>Hardware Interfacing</li></ul>	<ul style="list-style-type: none"><li>Near 100% automation of labor-intensive RF tests</li><li>Reduced test time from 16 Hours to 25 Minutes</li><li>Automatically generated results within 5 minutes</li></ul>

## PROCESSOR EXPERIENCE

### *Core*

- [TI ARM-Cortex] Tiva TM4C
- [TI 16-bit] MSP430 - 2-Series, 5-Series

### *Suppl*

- [TI ARM-Cortex] CC3200, CC2650
- [Silicon Labs] EFM8, EFM32
- [Atmel] AVR ATmega
- [Microchip] PIC32MX

## LANGUAGES

### *Core*

- C, Assembly (ARM, MSP430, PIC)
- JAVA

### *Experience With*

- C++
- Linux / Bash
- LabVIEW / MATLAB
- Swift / HTML

## TOPICS OF FIRMWARE EXPERIENCE

### *Central Skill & Passion*

- Deterministic, high-reliability firmware
- Low-latency interrupt response
- Firmware power consumption optimization
- Detailed & descriptive firmware
  - Clear & clean architecture
  - Complete documentation
- Strong firmware testing, design and report
  - Clear and detailed
  - Maximal automation and regression

### *Primary Skill*

- Firmware development with high portability and description
  - Clear, detailed and complete firmware architecture and documentation
  - Strong & uniform, repeatable firmware architecture and coding
- Communication protocol conformance and compliance
- Energy harvesting & battery-powered firmware architecture
- Assembly, C-Assembly co-existence

### *Topics of Prep (low-latency ramp)*

- RTOS
  - uCos-II
  - TI-RTOS

### *Deterministic Peripheral Usage*

- GPIO, ADC
- Timers, PWM
- XTAL, DCO, External Clocks
- Flash

### *Communication Peripherals*

- Core
  - SPI
  - UART (DB9)
  - RFID (18000-6C)
- Experience
  - Wi-Fi
  - Bluetooth
  - LAN
- Minimal Extension
  - USB
  - ZigBee

### *Light Experience*

- Embedded Linux

## TOPICS OF DESIGN EXPERIENCE

### *Core Topics of Work Experience*

- Manual communication protocol generation
- Protocol & Regulations Compliance
  - FIPS, ISO, SINIAV
- Firmware mapping, timing and floorplan
- Low-Power firmware
- Deterministic ISRs
- Lowest power paths to firmware task solution
- Low-power external peripheral usage

### *Design Topics of Strong Experience*

- Problem specification and solution architecture identification
- Prototyping and proving proposed new embedded system concepts
- PDRD & PRD generation
- Automated protocol test systems

### *Circuit Design & Fabrication Experience*

- PCB design (Circuit & layout)
- PCB manufacture, assembly, validation
- Experience with multiple design software packages
  - (Curr) Active Eagle experience, circuit design and board design
  - (2014) Prior Cadence experience
  - (2012) Prior Altium experience

### *Firmware Test & Measurement*

- Protocol compliance (protocol peripherals, automation, report generation)
- Firmware inspection, short-term & long-term test
  - USB DAQ, PCI-DAQ, NI PXIe-DAQ systems
  - LabVIEW interfaces, JAVA, CLI

### *Experience With*

- Architecture specification & design (System, firmware & hardware)
- Full lifecycle firmware operations (boot cycle to last cycle, knowledge and planning)
  - Failure analysis & mitigation (Design, test & validation)
- Mechatronics embedded-system design and implementation